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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/621,060
Filing Date: July 16, 2003
Appellant(s): HAALEN ET AL.

Eamon J. Wall
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 6-30-09 appealing from the Office action mailed 5-20-2009.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

GROUNDS OF REJECTION NOT ON REVIEW

The following grounds of rejection have not been withdrawn by the examiner, but they are not under review on appeal because they have not been presented for review in the appellant's brief.

- Claims 1-4, 6-9 and 11-16 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-4 of U.S. Patent No. 6,370,112 in view of Almay (US 5,809,011).
- Claims 5 and 10 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-4 of U.S. Patent No. 6,370,112 in view of Almay (US 5,809,011) and further in view of Merchant (US 6,535,489).

These rejections are set forth in final office action (mailed date 5/20/09) pages 8-17, and these rejection will not be present in section 9 below.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6667954	Boduch	12-2003
5809011	Almay	9-1998

6028861	Soirinsuo	2-2000
6535489	Merchant	3-2003
6370112	Voelker	4-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 6 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Boduch (US006667954B1).

Regarding Claim 1, Boduch discloses a communication network (see FIG. 1, redundant switching system 100), comprising:

at least two mutually different routing paths for commonly sourcing data packets (see FIG. 1, first path 105-111 and second path 106-112 for common source cells 103; see col. 3, line 36-67);

a switch (see FIG. 1, 2, Cell stream alignment best cell copy selection ASIC 110) having a plurality of inputs (see FIG. 1, received/input interfaces for paths 105-111 and 106-112)

respectively coupled to the routing paths for receiving the data packets (see FIG. 1, coupling to paths 105-111 and 106-112 for receiving packets/cells; see col. 4, line 1-40,44-53), and an output for forwarding the data packets (see FIG. 1, transmit/output interface of ASIC 110 for transmitting/forwarding the packets/cells; see col. 4, line 1-40,44-53);

the switch configured to discard or accept data packets depends on the source from which the data packet originates (**see FIG. 1, 2, discarding or transmitting/accepting packets/cells based/depends on the source/originator (*where the packets/cells originate*) (i.e. based on the source/originator who transmit a sequence number and identification number of the packet/cell which is used for discarding/transmitting; see col. 5, line 9-30, 50-65; see col. 6, line 30-60; see col. 8, line 40-50**);

wherein in response to a data packet being received out of order at a first of the plurality input ports (see FIG. 1,2, after receiving cells/packets out of sequence at the first receive/input interface 111; see col. 5, line 60 to col. 6, line 7), data packets received at the first input port are discarded for a period of time (see FIG. 2, sequence manager of AISC 110 drops the packet/cell, (e.g. by not writing into FIFO 204, or determining as bad cell), for that period of time; see col. 2, line 18-32; see col. 3, line 14-19; see col. 5, line 60 67; see col. 6, line 30-41,45-56; see col. 7, line 7-15, 33-44; see col. 8, line 35-40) while data packets received at the other input ports are processed (see FIG. 1,2, while/when receiving packets/cells at the second receive/input interface 112 by writing them into FIFO 204 for transmission; see col. 6, line 20-29,60 to col. 7, line 5, see col. 7, line 20-30; see col. 10, line 32 to col. 11, line 6) such that the data packets forwarded on the output are in correct order (see FIG. 1,2, so that packets/cells transmitted from the cell selector 206 at output/transmit interface of ASIC 110 is sequential order; see col. 10, line 32 to

col. 11, line 6) and further allow less of a number of bits to be forwarded than were transmitted (see col. 2, line 18-32; see col. 3, line 14-19; see col. 5, line 60 67; see col. 6, line 30-41,45-56; see col. 7, line 7-15, 33-44; see col. 8, line 35-40; allowing/selecting best copy of cell bits (note that ATM cell is 53 bytes/424 bits) for forwarding at the output/transmit interface than transmitted from input interface by discarding/dropping "not receiving" bad/out-of-sequence/copied cell bits thereby allowing/selecting the less number of cell bits to be transmitted; in other word, discarding cause the less number of cells/bits to be forwarded/allowed/selected than originally transmitted packets).

Regarding Claim 6, Boduch discloses a switch (see FIG. 1, 2, Cell stream alignment best cell copy selection ASIC 110) for use in a communication network (see FIG. 1, redundant switching system 100), the switch receiving data packets having a packet order (see FIG. 1,2, receiving packets/cells in a sequential order; see col. 4, line 1-40,44-53), determining whether the received data packets are in correct order (see FIG. 1, 2, determine/checking whether the received packets/cells are in a sequential order), and forwarding the received data packets in correct packet order (see FIG. 1, 2, transmitting/forward the received packet/cell in a proper sequential order; see col. 10, line 32 to col. 11, line 6), the switch comprising:

at least two incoming ports for receiving data packets (see FIG. 1, received/input interfaces/ports for paths 105-111 and 106-112 for receiving packets/cells) via respective routing paths (see FIG. 1, via paths 105-111 and 106-112; see col. 4, line 1-40,44-53) and an output port for forwarding data packets (see FIG. 1, transmit/output interface of ASIC 110 for transmitting/forwarding the packets/cells; see col. 4, line 1-40,44-53);

said data packets are discarded or accepted depending on the source form which the data packet originate (**see FIG. 1, 2, discarding or transmitting/accepting packets/cells based/depends on the source/originator (*where the packets/cells originate*) (i.e. based on the source/originator who transmit a sequence number and identification number of the packet/cell which is used for discarding/transmitting; see col. 5, line 9-30, 50-65; see col. 6, line 30-60; see col. 8, line 40-50**);

wherein in response to a commonly sourced data packet being received out of order at a first of the plurality input ports (see FIG. 1,2, after receiving cells/packets out of sequence at the first receive/input interface 111; see col. 5, line 60 to col. 6, line 7), commonly sourced data packets received at the first input port are discarded for a period of time (see FIG. 2, sequence manager of AISC 110 drops the packet/cell, (e.g. by not writing into FIFO 204, or determining as bad cell) while commonly sourced data packets received at the other input ports are processed (see FIG. 1,2, while/when receiving packets/cells at the second receive/input interface 112 by writing them into FIFO 204 for transmission; see col. 6, line 20-29,60 to col. 7, line 5, see col. 7, line 20-30; see col. 10, line 32 to col. 11, line 6) thereby allow less of a number of bits to be forwarded than were transmitted (see col. 2, line 18-32; see col. 3, line 14-19; see col. 5, line 60 67; see col. 6, line 30-41,45-56; see col. 7, line 7-15, 33-44; see col. 8, line 35-40; allowing/selecting best copy of cell bits (note that ATM cell is 53 bytes/424 bits) for forwarding at the output/transmit interface than transmitted from input interface by discarding/dropping "not receiving" bad/out-of-sequence/copied cell bits thereby allowing/selecting the less number of cell bits to be transmitted; in other word, discarding cause the less number of cells/bits to be forwarded/allowed/selected than originally transmitted packets).

Regarding Claim 11, Boduch discloses a switch (see FIG. 1, 2, Cell stream alignment best cell copy selection ASIC 110) for use in a communication network (see FIG. 1, redundant switching system 100), the switch receiving data packets having a packet order (see FIG. 1,2, receiving packets/cells in a sequential order; see col. 4, line 1-40,44-53), determining whether the received data packets are in correct order (see FIG. 1, 2, determine/checking whether the received packets/cells are in a sequential order), and forwarding the received data packets in correct packet order (see FIG. 1, 2, transmitting/forward the received packet/cell in a proper sequential order; see col. 10, line 32 to col. 11, line 6), comprising:

a plurality of input ports for successively receiving said data packets (see FIG. 1, received/input interfaces/ports for paths 105-111 and 106-112 for receiving packets/cells) from a respective plurality of routing paths (see FIG. 1, via paths 105-111 and 106-112; see col. 4, line 1-40,44-53); and

an output port for forwarding data packets (see FIG. 1, transmit/output interface of ASIC 110 for transmitting/forwarding the packets/cells; see col. 4, line 1-40,44-53);

said data packets are discarded or accepted depending on the source form which the data packet originate **(see FIG. 1, 2, discarding or transmitting/accepting packets/cells based/depends on the source/originator (*where the packets/cells originate*) (i.e. based on the source/originator who transmit a sequence number and identification number of the packet/cell which is used for discarding/transmitting; see col. 5, line 9-30, 50-65; see col. 6, line 30-60; see col. 8, line 40-50**);

wherein in response to a data packet being received out of order at a first of any one of the plurality input ports (see FIG. 1,2, after receiving cells/packets out of sequence at the first

receive/input interface 111; see col. 5, line 60 to col. 6, line 7), data packets are discarded for a period of time at the first input port (see FIG. 2, sequence manager of AISC 110 drops the packet/cell, (e.g. by not writing into FIFO 204, or determining as bad cell)) while being allowed at the other input ports (see FIG. 1,2, while/when receiving packets/cells at the second receive/input interface 112 by writing them into FIFO 204 for transmission; see col. 6, line 20-29,60 to col. 7, line 5, see col. 7, line 20-30; see col. 10, line 32 to col. 11, line 6) and thereby allowing less of a number of bits to be forwarded than were transmitted (see col. 2, line 18-32; see col. 3, line 14-19; see col. 5, line 60 67; see col. 6, line 30-41,45-56; see col. 7, line 7-15, 33-44; see col. 8, line 35-40; allowing/selecting best copy of cell bits (note that ATM cell is 53 bytes/424 bits) for forwarding at the output/transmit interface than transmitted from input interface by discarding/dropping "not receiving" bad/out-of-sequence/copied cell bits thereby allowing/selecting the less number of cell bits to be transmitted; in other word, discarding cause the less number of cells/bits to be forwarded/allowed/selected than originally transmitted packets).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 6-9, and 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Almay (US005809011A) in view of Soirinsuo (US006028861A).

Regarding Claim 1, Almay discloses a communication network (see FIG. 1, packet switch communication network), comprising:

at least two mutually different routing paths for commonly sourcing data packets (see FIG. 1, different/separate paths a-b and A-B for transmission of packets from common source node A (i.e. common souring data packets) since both paths a-b and A-B have common source Node A; see col. 2, line 33-50, see col. 3, line 10-26); and

a switch (see FIG. 1, Node B) having a plurality of inputs (see FIG. 1, received/input interfaces a-b and A-B) respectively coupled to the routing paths for receiving the data packets (see FIG. 1, coupling to a-b path and another interface from A-B path for receiving packets; see col. 2, line 38-67; see col. 4, line 20-35), and an output for forwarding the data packets (see FIG. 1, transmit/output interface of Node B for transmitting/forwarding the packets; see col. 1, line 31-36; col. 2, line 56 to col. 3, line 50);

the switch configured to perform processing data packet depending on the source from which the data packets originate (**see FIG. 1, Node B performing processing of packets depending/based on the source node A, where node A transmits packet at different time or Node A transmit re-route notification; see col. 3, line 1-60**);

wherein in response to a data packet being received at a first of the plurality input ports (see FIG. 1,2, after receiving cells/packets from source node A at the first input interface a-b; see col. 2, line 35-66; see col. 3, line 30 to col. 4, line 20), data packets received at the first input port are wait/hold for a period of time (see FIG. 2, col. 2, line 56 to col. 3, line 10; deactivating/ceasing/holding packets/cells from Node A at the first interface a-b for predetermined period) while data packets received at the other input ports are processed (see

FIG. 2, while/when receiving packets/cells from Node A at the second interface A-B; see col. 3, line 1-60) such that the data packets forwarded on the output are in correct order (see FIG. 1, routing the received packet in a correct/proper order (i.e. note that a correct/proper order of packets is formed when nodes A and B deactivating the route a-b for a predetermined time then activating the route A-B) via an output interface of node B; see col. 1, line 31-36; col. 2, line 56 to col. 3, line 50).

Almay does not explicitly disclose "out of order", "discard or accept" data packets, and "allow less of a number of bits to be forwarded than were transmitted".

However, receiving packets/cells/frames out of order due to changing network condition such as unavailable/fail/congested path and discarding the discarding out of order cells packets/cells/frames received at the port/interface in order to maintain network integrity is so well know in the art. In particular, Soirinsuo teaches a switch (see FIG. 8, 11, Switch) having a plurality of inputs for receiving the data packets (see FIG. 8, 11, input channels ports 1104 for receiving cells/packets), and an output for forwarding the data packet (see FIG. 8, 11, output channel port 1106 for route/forward the packets/cells; see col. 9, line 20-35; see col. 10, line 29-46);

the switch configured to discard or accept data packet depending on the source from which the data packets originate (**see FIG. 8, 9, 11, discarding or forwarding packets/cells depends/based on the originator/source switch who sends packets with last cell indication set (i.e. AUU or signaling) with associated cell identification VPI/VCI; last cell indication set cause the switchover to discard, non-last cell indication does not cause the switchover; see col. 9, line 1-30, 50-65; see col. 10, line 5-25**);

wherein in response to a data packet being received out of order at a first of the plurality input ports (see FIG. 8,11, upon receiving changed cells/packets which are "not" received in the same order in which they are transmitted due to network change path/routing (e.g. failure/congestion) at the first normal input port of 1104; see col. 9, line 20-35), data packets received at the first input port are discarded for a period of time (see col. 9, line 40-45; see col. 10, line 10-30; all cells received at the first/normal/old channel port 1104 are discarded during switch-over interval/time) while data packets received at the other input ports are processed (see col. 10, line 10-30, while/during receiving (and transmitting to the output port) from the new channel port), such that the data packets forwarded on the output are in correct packet order (see FIG. 8, 11, the packets/cells are transmitted/forwarded on the output channel port 1106 in the same proper/accurate order (i.e. the order as if the packets/cells are not lost due to failure/congestion); see col. 9, line 20-35; see col. 10, line 29-46) and further allow less of a number of bits to be forwarded than were transmitted (see col. 9, line 20-45; see col. 10, line 10-30; allowing/enabling the less number of cell bits (i.e. ATM cell is 53 bytes/424 bits) to forward to the output port than cell bits transmitted by the input port by discarding all cells received at the first/normal/old channel port 1104 during switch-over interval/time).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "discard or accept, out of order and allow less of a number of bits to be forwarded than were transmitted", as taught by Soirinsuo in the system of Almay, so that it would provide synchronize switchover and prevent frame integrity; see Soirinsuo col. 3, line 65 to col. 4, line 65.

Regarding Claim 2, the combined system of Almay and Soirinsuo discloses all claimed limitations. In particular, Almay discloses in response to a commonly sourced data packet being received at a second of the plurality input ports (see FIG. 2, when receiving packets/cells at the second interface A-B; see col. 3, line 1-60), commonly sourced data packets received at all of the input ports are hold/wait for a period of time (see FIG. 2, col. 2, line 56 to col. 3, line 10; deactivating/ceasing packets/cells at the first interface a-b or other interfaces (since ATM node can have more than two interfaces, see Almay col. 5, line 1-16; see col. 2, line 35-66; see col. 3, line 30 to col. 4, line 20).

Soirinsuo teaches in response to a commonly sourced data packet being received out of order at a second of the plurality input ports (see FIG. 8,11, upon receiving changed cells/packets which are "not" received in the same order in which they are transmitted due to network change path/routing (e.g. failure/congestion) at the second normal input port of 1104; see col. 9, line 20-35), commonly sourced data packets received at all of the input ports are discarded for a period of time (see col. 9, line 40-45; see col. 10, line 10-30; all cells received at the second/normal/old channel port 1104 are discarded during switch-over interval/time) while commonly sourced data packets received at the other input ports are processed (see col. 10, line 10-30, while/during receiving (and transmitting to the output port) from the new/first channel port).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide discarding and out of order, as taught by Soirinsuo in the system of Almay, so that it would provide synchronize switchover and prevent frame integrity; see Soirinsuo col. 3, line 65 to col. 4, line 65.

Regarding Claim 3, Almay discloses the period of time lasts until the switch is informed that re-ordering of the commonly sourced data packets is no longer possible (see col. 3, line 1-50; predefined period is defined such that ordering of packets at the new route connection that transmit cells/packets from possible and not disrupted. Since the predefined time last until the "ordering" of packet is "possible/not-disrupted", and thus "re-ordering" of packets are "not possible/disrupted").

Regarding Claim 4, Almay discloses the period of time has a predetermined length of time (see FIG. 2, col. 2, line 56 to col. 3, line 10; deactivating/ceasing packets/cells from subscriber A at the first interface a-b for predetermined period). Soirinsuo also discloses the period of time has a predetermined length of time (see FIG. 8, 11, first/normal connection/port; see col. 9, line 40-45; see col. 10, line 10-30; discarding all cells received from first/normal connection/port from the input source during switch-over interval/time).

Regarding Claim 6, Almay discloses a switch (see FIG. 1, 3, Node B) for use in a communication network (see FIG. 1, packet switch communication network), the switch receiving data packets having a packet order (see FIG. 1,3, receiving packets in a correct/proper order of packets), determining whether the received data packets are in correct order (see FIG. 1, 3, determine/checking whether the received packets are in a correct/proper order), and forwarding the received data packets in correct packet order (see FIG. 1, 3, routing/forward the received packet from source node A in a correct/proper order (i.e. note that a correct/proper order of packets is formed when nodes A and B deactivating the route a-b for a predetermined time then activating the route A-B); see col. 1, line 31-36; col. 2, line 56 to col. 3, line 50), the switch comprising:

at least two incoming ports for receiving data packets (see FIG. 1, two input interfaces to Node B receiving packets) via respective routing paths (see FIG. 1, via different/separate paths a-b and A-B; see col. 2, line 33-67; see col. 4, line 20-35) and an output port for forwarding data packets (see FIG. 1, 3, and output interface of Node B for routing packets; col. 2, line 56 to col. 3, line 50);

said data packets are processed depending on the source from which the data packet originate (**see FIG. 1, Node B performing processing of packets depending/based on the source node A, where node A transmits packet at different time or Node A transmit re-route notification; see col. 3, line 1-60**);

wherein in response to a commonly sourced data packet being received at a first of the plurality input ports (see FIG. 1,2, after receiving cells/packets from source node A at the first input interface a-b; see col. 2, line 35-66; see col. 3, line 30 to col. 4, line 20), commonly sourced data packets received at the first input port are wait/hold for a period of time (see FIG. 2, col. 2, line 56 to col. 3, line 10; deactivating/ceasing/holding packets/cells from Node A at the first interface a-b for predetermined period) while commonly sourced data packets received at the other input ports are processed (see FIG. 2, while/when receiving packets/cells from Node A at the second interface A-B; see col. 3, line 1-60).

Almay does not explicitly disclose “out of order”, “discard or accept” data packets, “allow less of a number of bits to be forwarded than were transmitted".

However, receiving packets/cells/frames out of order due to changing network condition such as unavailable/fail/congested path and discarding the discarding out of order cells packets/cells/frames received at the port/interface in order to maintain network integrity is so

well know in the art. In particular, Soirinsuo teaches a switch (see FIG. 8, 11, Switch) comprising at least two incoming ports for receiving the data packets (see FIG. 8, 11, the input channels ports 1104 for receiving cells/packets) and an output port for forwarding data packets (see FIG. 8, 11, output channel port 1106 for routing cells/packets; see col. 9, line 20-35; see col. 10, line 29-46);

said data packets are discarded or accepted depending on the source from which the data packet originate (**see FIG. 8, 9, 11, discarding or forwarding packets/cells depends/based on the originator/source switch who sends packets with last cell indication set (i.e. AUU or signaling) with associated cell identification VPI/VCI; last cell indication set cause the switchover to discard, non-last cell indication does not cause the switchover; see col. 9, line 1-30, 50-65; see col. 10, line 5-25);**

wherein in response to a commonly sourced data packet being received out of order at a first of the plurality input ports (see FIG. 8,11, upon receiving changed cells/packets which are "not" received in the same order in which they are transmitted due to network change path/routing (e.g. failure/congestion) at the first normal input port of 1104; see col. 9, line 20-35), commonly sourced data packets received at the first input port are discarded for a period of time (see col. 9, line 40-45; see col. 10, line 10-30; all cells received at the first/normal/old channel port 1104 are discarded during switch-over interval/time) while commonly sourced data packets received at the other input ports are processed (see col. 10, line 10-30, while/during receiving (and transmitting to the output port) from the new channel port), thereby allowing less of a number of bits to be forwarded than were transmitted (see col. 9, line 20-45; see col. 10, line 10-30; allowing/enabling the less number of cell bits (i.e. ATM cell is 53 bytes/424 bits) to

forward to the output port than cell bits transmitted by the input port by discarding all cells received at the first/normal/old channel port 1104 during switch-over interval/time).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "discard or accept, out of order, allow less of a number of bits to be forwarded than were transmitted", as taught by Soirinsuo in the system of Almay, so that it would provide synchronize switchover and prevent frame integrity; see Soirinsuo col. 3, line 65 to col. 4, line 65.

Regarding Claim 11, Almay discloses a switch (see FIG. 1, 3, Node B) configured for receiving data packets having a packet order (see FIG. 1,3, receiving packets in a correct/proper order of packets), determining whether the received data packets are in correct order (see FIG. 1, 3, determine/checking whether the received packets are in a correct/proper order), and forwarding the received data packets in correct packet order (see FIG. 1, 3, routing/forward the received packet from source node A in a correct/proper order (i.e. note that a correct/proper order of packets is formed when nodes A and B deactivating the route a-b for a predetermined time then activating the route A-B); see col. 1, line 31-36; col. 2, line 56 to col. 3, line 50), comprising:

a plurality of input ports for successively receiving said data packets (see FIG. 1, two input interfaces to Node B receiving packets) from a respective plurality of routing paths (see FIG. 1, from different/separate paths a-b and A-B; see col. 2, line 33-67; see col. 4, line 20-35); and

an output port for forwarding data packets (see FIG. 1, 3, and output interface of Node B for routing packets; col. 2, line 56 to col. 3, line 50);

said data packets are processed depending on the source from which the data packet originate (**see FIG. 1, Node B performing processing of packets depending/based on the source node A, where node A transmits packet at different time or Node A transmit re-route notification; see col. 3, line 1-60**);

wherein in response to a data packet being received at a first of any one of the plurality input ports (see FIG. 1,2, after receiving cells/packets from source node A at the first input interface a-b; see col. 2, line 35-66; see col. 3, line 30 to col. 4, line 20), data packets are wait/hold for a period of time at the first input port (see FIG. 2, col. 2, line 56 to col. 3, line 10; deactivating/ceasing/holding packets/cells from Node A at the first interface a-b for predetermined period) while being allowed at the other input ports (see FIG. 2, while/when receiving packets/cells from Node A at the second interface A-B; see col. 3, line 1-60).

Almay does not explicitly disclose “out of order”, “discard or accept”, “allow less of a number of bits to be forwarded than were transmitted".

However, receiving packets/cells/frames out of order due to changing network condition such as unavailable/fail/congested path and discarding the discarding out of order cells packets/cells/frames received at the port/interface in order to maintain network integrity is so well know in the art. In particular, Soirinsuo teaches a switch (see FIG. 8, 11, Switch) comprising a plurality of input ports for successively receiving said data packets (see FIG. 8, 11, the input channels ports 1104 for receiving cells/packets); and

an output port for forwarding data packets (see FIG. 8,11, output channel port 1106 for routing cells/packets; see col. 9, line 20-35; see col. 10, line 29-46);

said data packets are discarded or accepted depending on the source from which the data packet originate (**see FIG. 8, 9, 11, discarding or forwarding packets/cells depends/based on the originator/source switch who sends packets with last cell indication set (i.e. AUU or signaling) with associated cell identification VPI/VCI; last cell indication set cause the switchover to discard, non-last cell indication does not cause the switchover; see col. 9, line 1-30, 50-65; see col. 10, line 5-25);**

wherein in response to a data packet being received out of order at a first of any one of the plurality input ports (see FIG. 8,11, upon receiving changed cells/packets which are "not" received in the same order in which they are transmitted due to network change path/routing (e.g. failure/congestion) at the first normal input port of 1104; see col. 9, line 20-35), data packets are discarded for a period of time at the first input port (see col. 9, line 40-45; see col. 10, line 10-30; all cells received at the first/normal/old channel port 1104 are discarded during switch-over interval/time) while being allowed at the other input ports (see col. 10, line 10-30, while/during receiving (and transmitting to the output port) from the new channel port), thereby allowing less of a number of bits to be forwarded than were transmitted (**see col. 9, line 20-45; see col. 10, line 10-30; allowing/enabling the less number of cell bits (i.e. ATM cell is 53 bytes/424 bits) to forward to the output port than cell bits transmitted by the input port by discarding all cells received at the first/normal/old channel port 1104 during switch-over interval/time**).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "discard or accept, out of order, allow less of a number of bits to be forwarded than were transmitted", as taught by Soirinsuo in the system of Almay, so that it

would provide synchronize switchover and prevent frame integrity; see Soirinsuo col. 3, line 65 to col. 4, line 65.

Regarding Claim 7, the claim, which has disclosed all the limitations of the respective claim 2. Therefore, it is subjected to the same rejection as set forth above in claim 2.

Regarding Claim 8, the claim, which has disclosed all the limitations of the respective claim 3. Therefore, it is subjected to the same rejection as set forth above in claim 3.

Regarding Claim 9, the claim, which has disclosed all the limitations of the respective claim 4. Therefore, it is subjected to the same rejection as set forth above in claim 4.

Regarding Claim 12, Soirinsuo discloses wherein the data packets are forwarded without the discarded data packets received at the first of the input ports (see FIG. 8, 11, packets/cells are routed/forwarded without discarded cells/packets received at the first input channel port 1104; note that since the received packets/cells are discarded at the first input channel port 1104, and thus the discarded packets/cells are not forward/routed; see col. 10, line 25-45).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the data packets are forwarded without the discarded data packets received at the first of the input ports, as taught by Soirinsuo in the system of Almay, so that it would provide synchronize switchover and prevent frame integrity; see Soirinsuo col. 3, line 65 to col. 4, line 65.

Regarding Claim 13, Almay discloses wherein the period of time is a predetermined period of time (see FIG. 2, a time is a predefined period of time; see col. 3, line 1-15).

Regarding Claim 14, Almay discloses wherein the period of time is terminated in response to a determination that a data packet condition is no longer possible (see FIG. 2, predetermined time period has elapsed/terminated when determining that receiving packet state/condition impossible since the a-b line/path is deactivated; see col. 3, line 10-30). Soirinsuo also discloses wherein the period of time is terminated in response to a determination that a data packet condition is no longer possible (see col. 10, line 25-30; the switch-over interval/time is terminated/ended after all packets/cells are discarded which causes the packet status/condition no longer possible).

Regarding Claim 15, Soirinsuo discloses discard data packets for a period of time at all input ports apart from a single input (see col. 9, line 40-45; see col. 10, line 10-30; discarding all cells for a switch-over interval/time at the first/normal/old channel port 1104 apart from the second/new input channel port 1104) where data packets are determined to be arriving in the correct order (see FIG. 8, where cells/packets are received in the same order in which they are transmitted (i.e. correct order); see col. 9, line 20-35, 40-45; see col. 10, line 10-30).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide discarding data packets for a period of time at all input ports apart from a single input where data packets are determined to be arriving in the correct order, as taught by Soirinsuo in the system of Almay, so that it would provide synchronize switchover and prevent frame integrity; see Soirinsuo col. 3, line 65 to col. 4, line 65.

Regarding Claim 16, Soirinsuo discloses wherein only data packets the single input where data packets are determined to be arriving in the correct order are forwarded (see col. 9, line 40-45; see col. 10, line 10-30; cell/packets in the new/second input channel where

cells/packets are receiving/arriving in the same order in which they are transmitted (i.e. correct order) are forwarded/routed).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide only data packets the single input where data packets are determined to be arriving in the correct order are forwarded, as taught by Soirinsuo in the system of Almay, so that it would provide synchronize switchover and prevent frame integrity; see Soirinsuo col. 3, line 65 to col. 4, line 65.

5. Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Almay in view of Soirinsuo as applied to claims 1 and 6 above, and further in view of Merchant (US006535489B1).

Regarding Claims 5 and 10, the combined system of Almay and Soirinsuo discloses the communication network as set forth above in claims 1 and 6.

Neither Almay nor Soirinsuo explicitly disclose "an Ethernet Network".

However, utilizing Ethernet 802.3 network is well known in the art in order to provide a standard connection for interoperability. In particular, Merchant discloses an Ethernet network (see FIG. 1, Ethernet 802.3 network; see col. 3, line 45-65).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide Ethernet network, as taught by Merchant, in the combined system of Almay and Soirinsuo, so that it would enable selectively forwarding data packets to appropriate destination based on Ethernet protocol; see Merchant col. 3, line 60-65.

(10) Response to Argument

A. GROUND OF REJECTION 1 (Claim 1, 6 and 11)

A.1. Claim 1.

The Appellants argued that, "…

(i) Boduch fails to teach or suggest … "the switch *configured to discard or accept data packets depending on the source from which the data packet originates"…*

(ii) Selecting "the better of two or more copies of cells" is not equivalent to the claimed discarding", wherein cells are irrevocably prevented from being forwarded, as exemplified among other places in the *Appellants' FIG. 10, wherein cells 1, 3 and 4 are forwarded, and cell 2 is discarded with destination B not receiving a copy of a cell; thereby allowing fewer (i.e. less of a number of bits) to be forwarded than were transmitted....*

(iii) Boduch does not even *allow fewer bits to be forward than were transmitted*, on contrast to the claimed "discarding"

(iv) Boduch failing to teach "discarding", the reference also fails to teach or suggest the claimed "data packets forwarded on the output are in the correct packet order";

(v) By "sequential order", Boduch is not referring to *packets being in the same order as they were originally transmitted*…The sequence number is arbitrarily assigned to all cells at the receiving end (ASIC 110) of the system, based on incremental order in which they arrive, not with respect to the order in which they are transmitted

(vi) Boduch does not teach or suggest "*in response to a data packet being received out of order at a first of the plurality input ports, data packets received at the other input ports are*

processed, such that the data packet forwarded on the output are in correct packet order" in pages 10-12.

In response to Appellants argument, t**he examiner respectfully disagrees** with the argument above.

In response to Appellants argument in sub-section (i), (iv) and (vi), Boduch discloses the switch configured to discard or accept data packets depends on the source from which the data packet originate (**see FIG. 1, 2, discarding or transmitting/accepting packets/cells based/depends on the source/originator (*where the packets/cells originate*) (i.e. based on the source/originator who transmit a sequence number and identification number of the packet/cell which is used for discarding/transmitting; see col. 5, line 9-30, 50-65; see col. 6, line 30-60; see col. 8, line 40-50**).

wherein in response to a data packet being received out of order at a first of the plurality input ports (**see FIG. 1,2, after receiving cells/packets out of sequence at the first receive/input interface 111; see col. 5, line 60 to col. 6, line 7**), data packets received at the first input port are discarded for a period of time (**see FIG. 2, sequence manager of AISC 110 drops the packet/cell, (e.g. by not writing into FIFO 204, or determining as bad cell), for that period of time; see col. 2, line 18-32; see col. 3, line 14-19; see col. 5, line 60 67; see col. 6, line 30-41,45-56; see col. 7, line 7-15, 33-44; see col. 8, line 35-40**) while data packets received at the other input ports are processed (**see FIG. 1,2, while/when receiving packets/cells at the second receive/input interface 112 by writing them into FIFO 204 for transmission; see col. 6, line 20-29,60 to col. 7, line 5, see col. 7, line 20-30; see col. 10, line 32 to col. 11, line 6**) such that the data packets forwarded on the output are in correct order (**see**

FIG. 1,2, so that packets/cells transmitted from the cell selector 206 at output/transmit interface of ASIC 110 is sequential order; see col. 10, line 32 to col. 11, line 6), and further allow less of a number of bits to be forwarded than were transmitted (**see col. 2, line 18-32; see col. 3, line 14-19; see col. 5, line 60 67; see col. 6, line 30-41,45-56; see col. 7, line 7-15, 33-44; see col. 8, line 35-40; allowing/selecting best copy of cell bits (note that ATM cell is 53 bytes/424 bits) for forwarding at the output/transmit interface than transmitted from input interface by discarding/dropping "not receiving" bad/out-of-sequence/copied cell bits thereby allowing/selecting the less number of cell bits to be transmitted**; *in other word, discarding cause the less number of cells/bits to be forwarded/allowed/selected than originally transmitted packets*).

Thus, it is clear that Boduch clearly discloses the Appellants broadly claimed invention.

In response to Appellants argument on subsection (ii) and (v) that the references fail to show certain features of Appellants invention, it is noted that the features upon which Appellants relies (i.e., (1) *Appellants' FIG. 10, wherein cells 1, 3 and 4 are forwarded, and cell 2 is discarded with destination B not receiving a copy of a cell; thereby allowing fewer (i.e. less of a number of bits) to be forwarded than were transmitted; and(2) packets are transmitted in sequential order; (3) allow fewer bits to be forward than were transmitted*) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). In this case, it is clear that none of the specific detailed of Appellants FIG. 10 and its corresponding detailed limitations are recited in the claimed. Moreover, the broad claim does not even recite that "*packets are transmitted in sequential*

order" or "allow "fewer bits to be forward than were transmitted". Thus, arguments based on limitations that are not disclosed in the BROAD claimed invention is irrelevant.

In response to Appellants argument on subsection (ii), Appellants **admits on the record** (in attempt to overcome 35 U.S.C. 112, first paragraph rejection) that such claimed invention limitations are **well known in the art**. In particular, per Appellants remark, page 6, filed 3-27-09, which states "*allow less of a number of bits to be forwarded than were transmitted"* is disclosed as "*data packets 1, 2, 3, 4 were originally transmitted, however, only data packet packets 1, 3, 4 arrives at destination B*" which is well known in the art. **Additionally, Appellants also admits that the invention is well known in the art since** "There is no experimentation required by the average individual because an artisan of ordinary skill in the art would easily comprehend the above-referenced disclosure. Without a reasonable basics of questioning the adequacy of disclosure to enable a person of ordinary skill in the art to make and use the claimed invention."

In response to Appellants argument, at one instant in the prosecution, in attempt to overcome 35 U.S.C. 112, first paragraph rejection, the Appellants admits that such detailed disclosure is not required to recited in the specification since it is so well known in the art that *an artisan of ordinary skill in the art would easily comprehend the above-referenced disclosure.* In other word, make and use of such limitation so well known in the art that Appellants is not even required to disclose them in detail in the original specification, in which examiner agrees.

However, at this last instant in the prosecution, Appellants is now arguing that such limitation is not well known or obvious to a person of ordinary skill in the art, by attacking the prior art for not disclosing such well known features.

Thus, it is clear that Appellants is switching the position on every instant of the prosecution. Thus, such arguments presented by the Appellants based on uncertain Appellants position are clearly an error.

In response to Appellants argument on subsection (ii, iii, iv) based on "discarding", Boduch discloses as follows:

In particular, if the sequence manager 203 determines that the sequence number is not equal to the previous sequence number+1, or the initialization bit in the cell overhead is set, or initialization has been commanded by software, or a composite cell stream error has occurred, then the sequence manager 203 maintains the sequence status in the out of sequence state 301, reports a loss of sequence in the CDV FIFO status 207, **does not write the cell into CDV FIFO, and updates the previous sequence number with the value of the sequence number** of the current cell. (see col. 6, line 35-40)

If the sequence manager 203 begins in the sequence error state 303 and the conditions at block 305 exist, then the sequence manager 203 transitions the sequence state of that cell stream to the out of sequence state 301. In particular, if the sequence manager 203 determines that the sequence number is not equal to the previous sequence number+1, or the initialization bit in the cell overhead is set, or initialization has been commanded by software, or composite cell stream errors have occurred, t**hen the sequence manager 203 transitions the sequence status to the out of sequence state 301, reports a loss of sequence, does not write the cell into the CDV FIFO**, and updates the previous sequence number with the value of the sequence number of the current cell. (see col. 6, line 50-66)

Thus, it clear that when not writing the bad cell into memory/FIFO by updating the sequence number, it is the same as discarding the cell. For example, when deleting the file on Personal computer (PC), the deleted file is no longer re-stored/re-written in the memory, thereby deleting/discarding from the memory. Some scenario apply in this case, when the bad cell is not written to the FIFO/memory, it is discarded/deleted since it will no longer be stored. One cannot “physically” discard the data packet. Thus, it is clear that "discarding" is simply not writing the cell into FIFO/memory.

Boduch further discloses as follows:

A switch network which provides redundancy is comprised of two or more redundant switch network copies. Such a redundancy scheme provides a vehicle whereby the "better" (also sometimes characterized in the art as the "best") cell of two or more copies of a cell may be selected for insertion into the data stream. Providing at least two redundant or competing cell streams from which to choose the better cell, **as determined based upon at least one measure of cell quality, ensures the integrity of the data and minimizes the number of cells that may be dropped as "bad."** (see col. 1, lines 40-49)

The present invention relates to methods and apparatus for selecting the better of two or more copies of any given cell from the received cell streams, **dropping the least number of cells, while maintaining the ordered nature of the cell stream.** The two or more copies of a cell presented for selection originate from multiple redundant switch network copies. These cell copies move through a redundant switch network, where the best cell copy selection is made, and the selected cell copy is inserted into the data stream. (see col. 2, line 26-36)

Cells may be received at non-regular intervals from the redundant switch network copies, or one or more cells may be dropped entirely. However, the CDV FIFO collection 402 must be able to absorb this delay variation in order to pass along cells at regular intervals. (see col. 8, line 35-40)

In view of the above, it is clear that Boduch discloses "dropping" or "discarding" the cell that are bad.

In response to Appellants argument on subsection (v), Boduch clearly disclose outputting the correct packet number by utilizing the sequence manager as set forth above. Again, the arguments based on whether Bouduch "***transmits packet in order***" or "***arrive with respect to the order in which they are transmitted***" is irrelevant, since these limitations are being claim. Even if these limitations were required to consider, Boduch clearly discloses them as set forth above.

A.2. Claim 6 and 11.

The Appellants argued that, "…

(i) Appellants initially shows error in the rejection of claim 6 and 11 in that in the office action the examiner lumped claims 1, 6 and 11 together and only address the limitations of claim 1; therefore the limitations of claim 6 and 11 that are different from claim 1 have not been addressed…the rejection is not equally applicable to all the claims in the group because claim 6 recites, "at least two ports for receiving data packets via respective routing paths and an output port for forwarding data packets" limitation whereas claim 1 does not…

(ii) Claims 6 and 11 further recites: "*said data packets are discarded or accepted depending on the source from which the data packets originate*". As articulated above with respect to claim 1, Boduch does not disclose this claimed feature...Boduch does not anticipated claims 6 and 11..." pages 12-13.

In response to Appellants argument, t**he examiner respectfully disagrees** with the argument above.

In response to Appellants argument on subsection (i), **nowhere** in the final rejection (mailed 5-20-09), the claims 1, 6 and 11 are lumped together. In particular, examiner was unable to find any portion in the final action where claims 1, 6 and 11 are grouped/lumped together and only address the limitation of claim 1. The arguments are clearly an error since there are no facts supporting this. If Appellants still disagree, examiner hereby requests the Appellants to identify where in the final action where these claims are allegedly grouped/lumped.

In response to Appellants argument on subsection (ii), since these arguments are based on claim 1, please see the response to claim 1 set forth above.

In view of the above, it is clear that both claims 6 and 11 are also anticipated by Boduch.

A. GROUND OF REJECTION 2 (Claim 1-4, 6-9 and 11-16)

B.1. Claim 1.

The Appellants argued that, "…

(i) the office action failed to establish a prima facie case of obviousness because the combination of Almay and Soirinsuo fails to teach or suggest all the claim elements... the invention claims "*in response to a commonly sourced data packet being received out of order at a first of the plurality of input ports, commonly sourced data packets received at the first input port are discarded for a period of time while commonly sourced data packets received at the other input port are processed said data packet are discarded or accepted depending on the source from which the data packets originate*"

(ii) Soirinsuo never allows data at any more than input port to be consider, or "processed" at any given time

(iii)Even though Soirinsuo mention the word "discard", the Appellants respectfully maintain that the art distinctly teach away from "discard" as specifically claimed.

(iv) Soirinsuo does not mention any provision for actually detecting if packets are cells are being received out of order or not, so for one, it is not even possible for Soirinsuo to specifically respond "to a commonly sourced data packet being received out of order" by any means.

(v) examiner latches to one word "discard" and ignore the remainder of the limitation in its entirety, to wit, "said data packets are discarded or accepted depending on the source from which the data packets originate"…the present of the individual letters in a reference does not mean that the initial claim term has been disclosed or suggested" page 13-15.

In response to Appellants argument, **the examiner respectfully disagrees** with the argument above.

In response to Appellants arguments, on subsection (i) and (v), against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, the rejection is based on the combined system of Almay and Soirinsuo as set forth above, and thus one must consider the combination of system.

In particular, Almay discloses the switch configured to perform processing data packet depending on the source from which the data packets originate (**see FIG. 1, Node B performing processing of packets depending/based on the source node A, where node A transmits packet at different time or Node A transmit re-route notification; see col. 3, line 1-60**); wherein in response to a data packet being received at a first of the plurality input ports (**see FIG. 1,2, after receiving cells/packets from source node A at the first input interface a-b; see col. 2, line 35-66; see col. 3, line 30 to col. 4, line 20**), data packets received at the first input port are wait/hold for a period of time (**see FIG. 2, col. 2, line 56 to col. 3, line 10; deactivating/ceasing/holding packets/cells from Node A at the first interface a-b for predetermined period**) while data packets received at the other input ports are processed (**see FIG. 2, while/when receiving packets/cells from Node A at the second interface A-B; see col. 3, line 1-60**) such that the data packets forwarded on the output are in correct order (**see FIG. 1, routing the received packet in a correct/proper order (i.e. note that a correct/proper order of packets is formed when nodes A and B deactivating the route a-b**

for a predetermined time then activating the route A-B) via an output interface of node B; see col. 1, line 31-36; col. 2, line 56 to col. 3, line 50), thereby allowing less of a number of bits to be forwarded than were transmitted (**see col. 9, line 20-45; see col. 10, line 10-30; allowing/enabling the less number of cell bits (i.e. ATM cell is 53 bytes/424 bits) to forward to the output port than cell bits transmitted by the input port by discarding all cells received at the first/normal/old channel port 1104 during switch-over interval/time**).

Soirinsuo discloses the switch configured to discard or accept data packet depending on the source from which the data packets originate (**see FIG. 8, 9, 11, discarding or forwarding packets/cells depends/based on the originator/source switch who sends packets with last cell indication set (i.e. AUU or signaling) with associated cell identification VPI/VCI; last cell indication set cause the switchover to discard, non-last cell indication does not cause the switchover; see col. 9, line 1-30, 50-65; see col. 10, line 5-25**); wherein in response to a data packet being received out of order at a first of the plurality input ports (**see FIG. 8,11, upon receiving changed cells/packets which are "not" received in the same order in which they are transmitted due to network change path/routing (e.g. failure/congestion) at the first normal input port of 1104; see col. 9, line 20-35)**, data packets received at the first input port are discarded for a period of time (**see col. 9, line 40-45; see col. 10, line 10-30; all cells received at the first/normal/old channel port 1104 are discarded during switch-over interval/time**) while data packets received at the other input ports are processed (**see col. 10, line 10-30, while/during receiving (and transmitting to the output port) from the new channel port**), such that the data packets forwarded on the output are in correct packet order (**see FIG. 8, 11, the packets/cells are transmitted/forwarded on the output channel port 1106 in the**

same proper/accurate order (i.e. the order as if the packets/cells are not lost due to failure/congestion); see col. 9, line 20-35; see col. 10, line 29-46) and further allow less of a number of bits to be forwarded than were transmitted (**see col. 9, line 20-45; see col. 10, line 10-30; allowing/enabling the less number of cell bits (i.e. ATM cell is 53 bytes/424 bits) to forward to the output port than cell bits transmitted by the input port by discarding all cells received at the first/normal/old channel port 1104 during switch-over interval/time**).

In response to Appellants arguments, on subsection (ii), Soirinsuo is not required to disclose "allows data at any more than input port to be consider, or "processed" at any given time" since these limitations have already been disclosed by Almay, and the rejection is based on a combination of system, not Soirinsuo alone. Although it is not required, Soirinsuo discloses the use of input channels ports and output channels ports as set froth above. Thus, the arguments are clearly an error.

(iii)Even though Soirinsuo mention the word "discard", the Appellants respectfully maintain that the art distinctly teach away from "discard" as specifically claimed.

In response to Appellants arguments, on subsection (iii) and (v), examiner is confused with the Appellants argument since Soirinsuo clearly discloses "discarding", yet Appellants argues that Appellants' "discarding" is not the same claimed "discarding". Examiner clearly provides the facts and evidence that Appellants "discarding" is clearly well known as disclosed in the prior art Soirinsuo. In fact, Soirinsuo clearly recites the identical word "discarding" as the claim limitation "discarding"; however, Appellants totally ignores the fact presented by the examiner. Soirinsuo discloses more than individual letters of "discarding".

In particular, Soirinsuo discloses as follows:

Another aspect of the present invention is that all cells coming from the second virtual channel link are discarded until a frame complete state is detected on the first virtual channel link.

Another aspect of the present invention is that all cells on the first virtual channel link are discarded after the frame completed state is detected on the first virtual channel link. (see col. 4, line 45-53).

For egress switch-over, the egress port will monitor the "new" channel after being notified about switch-over. Both incoming VCLs have a separate ATM layer identification, i.e., VPI/VCI and possibly a routing tag, at the outgoing side**. The switch will discard all cells coming from that connection until it receives a cell with AUU set**.

For an egress switch-over, the ATM switch will send out all cells coming from the "new" connection and **discard all cells received on the "old" channel**.

(see col. 10, line 10-16, and lines 25-29)

In view of the above, Soirinsuo disclose the functionality of discard which is more than a few letters.

In response to Appellants augment on subsection (iii), Soirinsuo's teaches the switch determines whether or not to discard the packet based upon the transmitter/sender/source where the cells originate, where the transmitter/sender/source uses the AUU or user signaling bit to set the indication of the last cell. Based on that cell with the AUU set, the switch-over occurs which triggers the discarding of cells as set forth above. Thus, it is clear that Soirinsuo teaches the amended limitation. **Examiner acknowledges Appellants admission of Soirinsuo reciting the text and invention of "discarding".** Since Soirinsuo clearly and precisely discloses the text for utilizing "**discarding**" in the invention as admitted by the Appellants, Soirinsuo does not teach away from "discard". Moreover, since **the exact claimed limitation "discarding"** is being disclosed in Soirinsuo, one skilled in the ordinary would clearly see that Soirinsuo clearly does not teach away.

B.2. Claims 6 and 11.

The Appellants argue that, "as articulated with respect to claim 1, there are missing claimed features not taught/suggested by the cited references…and thus, independent claim 6 and 11 have been erroneously rejected…" on page 15.

In response to Appellants argument, t**he examiner respectfully disagrees** with the argument above since the claim 1 clearly disclosed by the combined system as set forth above. Thus, please see the response set forth above in claim 1.

B.3. Claims 2-4, 7-9 and 12-16.

The Appellants argue that, "claims 2-4, 7-9 and 12-16 are patentable under 35 U.S.C 103(a) over Almay in view of Soirinsuo as applied to claims 1, 6 and 11 above……" on page 15.

In response to Appellants argument, t**he examiner respectfully disagrees** with the argument above since the claim 1 clearly disclosed by the combined system as set forth above. Thus, claims 2-4, 7-9 and 12-16 are still not patentable for the same reason as set forth in claims 1, 6 and 11. Thus, please see the response set forth above in claims 1, 6 and 11 above.

C.1. Claims 5 and 10.

The Appellants argue that, "claims 2-4, 7-9 and 12-16 are patentable under 35 U.S.C 103(a) over Almay in view of Soirinsuo as applied to claims 1, 6 and 11 above……" on page 15-16.

In response to Appellants argument, t**he examiner respectfully disagrees** with the argument above since the claim 1 clearly disclosed by the combined system as set forth above. Thus, claims 5 and 10 are still not patentable for the same reason as set forth in claims 1, 6 and 11. Thus, please see the response set forth above in claims 1, 6 and 11 above.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

Conclusion

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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